**Skyworks PCIe Clock Jitter Tool README**

**http://www.skyworksinc.com/ia/pcie-jittertool**

## PC System Requirements

Operating System:

The PCIe Clock Jitter Tool (PCIe Tool) requires a 64-bit version of Windows Vista, Windows 7, Windows 8, Windows 10, or Windows 11. 32-bit Windows is not supported due to memory requirements to process large amounts of data.

The PCIe Tool uses Microsoft.NET Framework version 4.5. The installer will check to see if it is installed and, if not, prompt to automatically download and install it.

If you need to install the PCIe Tool on a PC that does not have an Internet connection and does not have .NET 4.5, you can download Microsoft's stand-alone installer from http://download.microsoft.com/download/b/a/4/ba4a7e71-2906-4b2d-a0e1-80cf16844f5f/dotnetfx45_full_x86_x64.exe. Install .NET 4.5 before running the PCIe Tool installer.

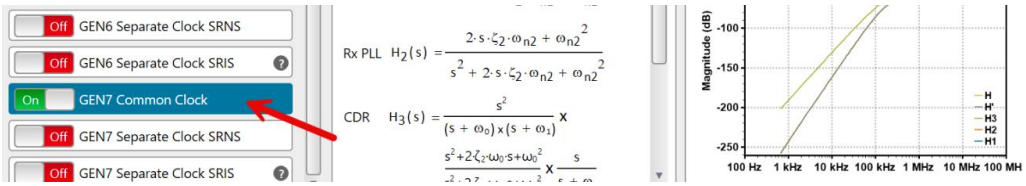
1024 x 768 screen resolution or greater

## Revision History

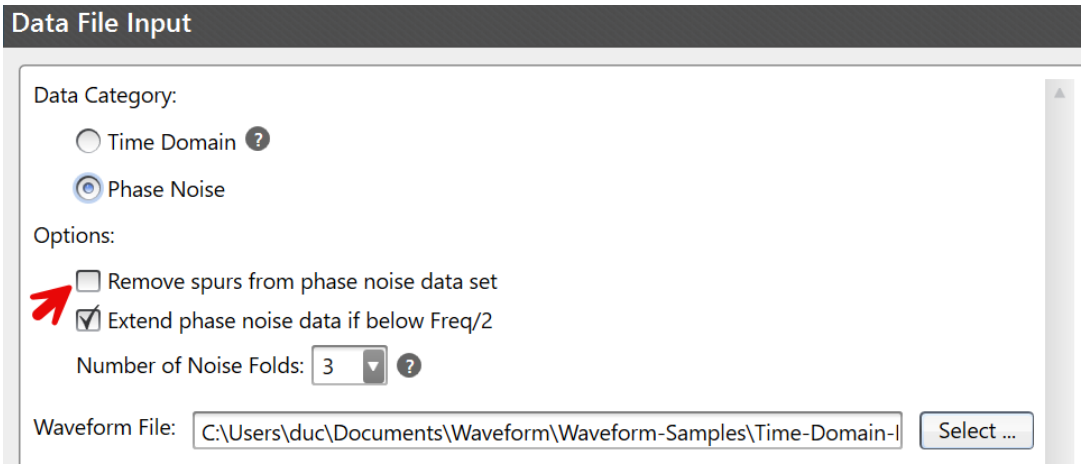
### Version 8.0 [2025-06-04]

Improvements:

- Added support for PCIe Gen 7 filters (PCI-Express Base Specification 7.0 rev. 1.0). (TMGSW-3601)




- Added SSC removal option for phase noise waveforms. (TMGSW-1302)




- Apply Spread Spectrum removal on R&S PN data when SS is on. (TMGSW-1302)
- In CSV data export, Omega and Zeta constants that are not applicable to a filter are now blank in a cell instead of "NaN". (TMGSW-3922)

**Transfer Function Constants**

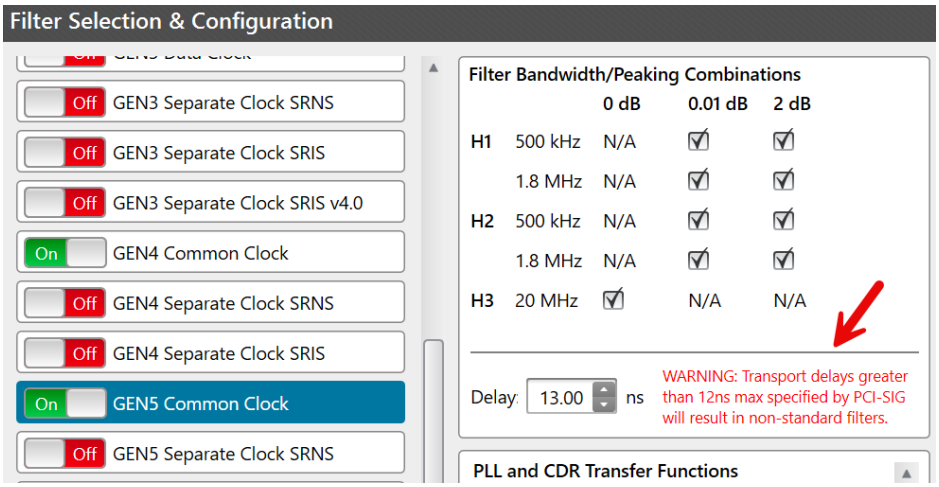
| # | Class | Architecture | Specs | H1 BW | H1 Peaking | H1 Omega | H1 Zeta | H2 BW | H2 Peaking | H2 Omega | H2 Zeta | H3 BW | H3 Peaking | H3 Omega | H3 Zeta | Delay |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GEN1 | Common Clock | 1.1<br>2.1<br>3.1 | 1.5 MHz | 3 dB | 5.06989E+6 | 5.40000E-1 | 1.5 MHz | 3 dB | 5.06989E+6 | 5.40000E-1 | 1.5 MHz | 0 dB | 9.42478E+6 | | 10 ns |
| 2 | GEN1 | Common Clock | 1.1<br>2.1<br>3.1 | 1.5 MHz | 3 dB | 5.06989E+6 | 5.40000E-1 | 22 MHz | 3 dB | 7.43584E+7 | 5.40000E-1 | 1.5 MHz | 0 dB | 9.42478E+6 | | 10 ns |
| 3 | GEN1 | Common Clock | 1.1<br>2.1<br>3.1 | 22 MHz | 3 dB | 7.43584E+7 | 5.40000E-1 | 22 MHz | 3 dB | 7.43584E+7 | 5.40000E-1 | 1.5 MHz | 0 dB | 9.42478E+6 | | 10 ns |
| 4 | GEN2 | Common Clock | 1.1<br>2.1<br>3.1 | 5 MHz | 0.5 dB | 8.30197E+6 | 1.75000E+0 | 16 MHz | 0.5 dB | 2.65663E+7 | 1.75000E+0 | | | | | 12 ns |
| 5 | GEN2 | Common Clock | 1.1<br>2.1<br>3.1 | 5 MHz | 0.5 dB | 8.30197E+6 | 1.75000E+0 | 16 MHz | 1 dB | 3.68944E+7 | 1.15000E+0 | | | | | 12 ns |

- Eliminate the 300mV limit and associated Pass/Fail for a differential signal and report only the measured numbers. (TMGSW-3565)

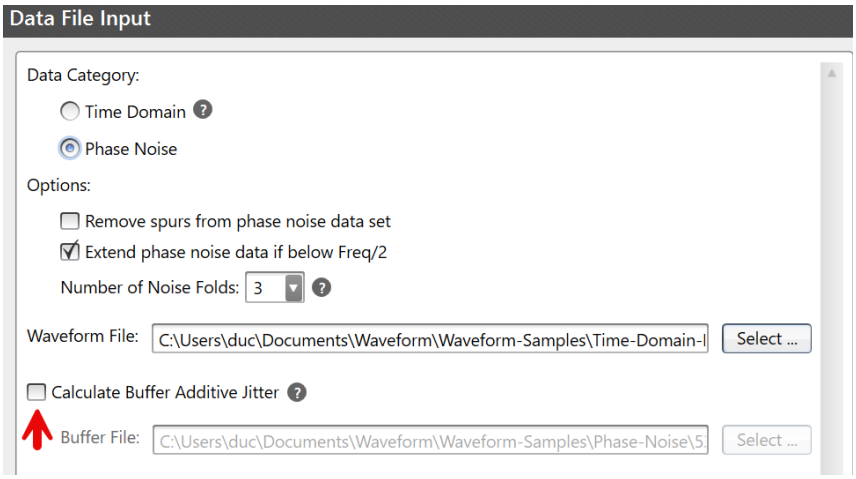
**Reference Clock AC Specifications**

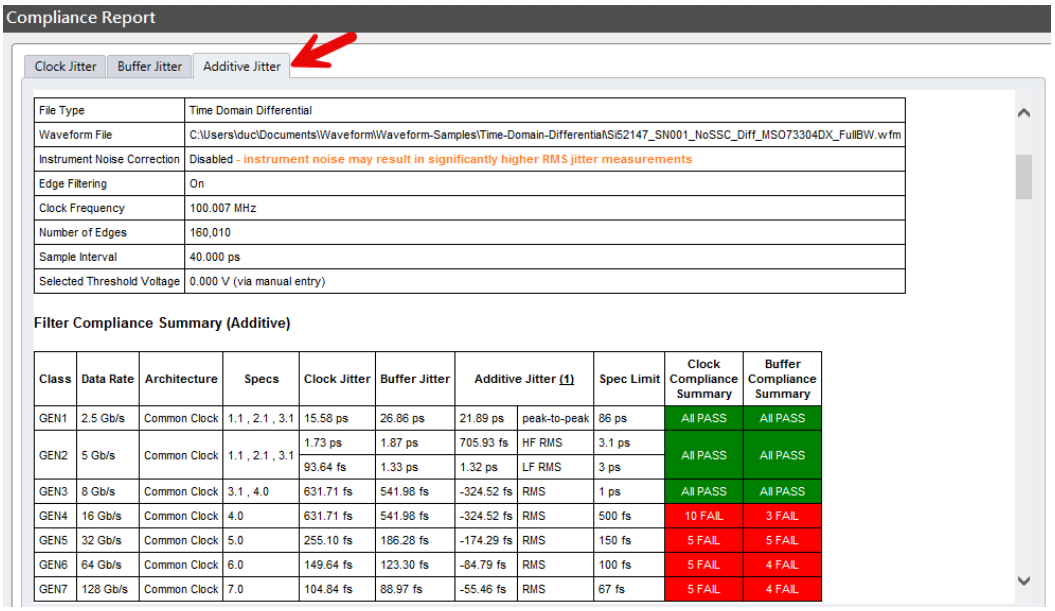
| Symbol | Parameter | Specification | | Analysis Result | | | Compliance Result |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Avg | |
| Rising Edge Rate | Rising Edge Rate | 0.6 V/ns | 4 V/ns | 1.45 V/ns | 1.66 V/ns | 1.55 V/ns | PASS |
| Falling Edge Rate | Falling Edge Rate | 0.6 V/ns | 4 V/ns | 1.39 V/ns | 1.58 V/ns | 1.48 V/ns | PASS |
| $V_{IH}$ | Differential Input High Voltage | 150 mV | | 376.76 mV | 403.40 mV | 390.60 mV | PASS |
| $V_{IL}$ | Differential Input Low Voltage | | -150 mV | -419.65 mV | -385.30 mV | -403.45 mV | PASS |
| $V_{RB}$ | Ring-Back Voltage | | 200 mV | N/A | 57.26 mV | 33.12 mV | PASS |
| $V_{OVS}$ | Overshoot Voltage relative to $V_{IH}$ | | | -13.834 mV | 15.754 mV | 0.249 mV | N/A |
| $V_{UDS}$ | Undershoot Voltage relative to $V_{IL}$ | | | -14.994 mV | 16.202 mV | 0.152 mV | N/A |

- Update transport delay to remove 12ns max limit and replace with warning. (TMGSW-1047)



- Added additive buffer jitter checkbox to the Data File Input screen to perform the RMS calculation between the clock and buffer jitter values. (TMGSW-1052)




## Version 7.1 [2022-12-15]

Improvements:

- Reduced limit for recommend minimum number of edges from 160000 to 100000. This does not effect calculations, only a warning that is displayed if the number of edges detected in the waveform is less than what is recommended in the PCIe specification.
- Removed note on PCIe 6.0 Base Specification pending final release.
- Added new --mode option to the PCIeDataCompare command line tool. Use to calculate additive jitter and to perform scope noise correction on data with spread spectrum. '--mode additive' will add an extra column containing the Root Subtraction of the squares of the buffer input and output RMS values. '--mode correction' will add two extra columns: one with the isolated scope noise RMS, and one for the corrected SS enabled RMS result.

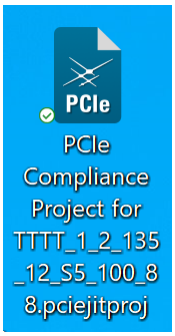
## Version 7.0 [2021-08-25]

Skyworks Solutions, Inc. has acquired the Infrastructure & Automotive (I&A) business from Silicon Labs. We truly appreciate your business and look forward to working together at Skyworks.

When the new Skyworks PCIe Clock Jitter tool is installed, it will prompt you to delete the Silicon Labs version if found on your PC. This is optional and not required should you need to use an older version of the tool. The two versions can co-exist and even run side-by-side on your PC.

The default extension for PCIe Clock Jitter Tool project files is now “pciejitproj”. When opening a project – which contains saved file, options, and filter sections – files with the old extension “slabpcieproj” will continue to be shown in the project open dialog and can still be saved with this extension.

You may need to log out or restart your PC to pick up the new extension mapping so that you can double click a pciejitproj extension file. If you see the new icon for your pciejitproj file, you should be good to go and can double click the project to automatically open it in the Skyworks PCIe Clock Jitter Tool.




## Version 6.2 [2021-06-25]

Fixed: eliminate VIL/VIH max/min failures in the Reference Clock AC Specifications table (TMGSW-2015)

## Version 6.1 [2021-05-06]

The Instrument Noise Correction (aka Scope Noise Removal) is out of Beta. In this release, there are no changes to the underlying removal algorithms. However, there are now warnings in the GUI and compliance reports prompting users to use this feature for time domain input. Doing so will correct for the RMS jitter contribution from your oscilloscope.

Other improvements:

- GEN2 RMS MAX RMS split into low and high frequency components
- Several new footnotes added to compliance report
- New noise folding section in the User’s Guide

## Version 6.0 [2021-01-14]

Improvements:

- Added Instrument Noise Correction (aka Scope Noise Removal) option (Beta); please review the new section in the User’s Guide for more information
- Added option to turn the edge smoothing filter ON or OFF
- Improved the edge smoothing filter algorithm
- Added double crossing warning to the Data File Overview section of the compliance report
- Added Min/Max boundaries to the waveform plot

## Version 5.0 [2020-05-20]

Improvements:

- Fixed: phase-domain SRIS/SRNS RMS jitter calculations were being scaled by sqrt(2)

- Added preliminary support for PCIe Gen 6 filters (PCI-Express Base Specification 6.0 rev. 0.5)
- Added SRNS/SRIS jitter limit for Gen5 and Gen6. This is provided as an informative measurement only. The limits were calculated based on the system simulation budget as described at https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/white-papers/PCIe-Clock-Source-Selection.pdf.
- In SRIS and SRNS, both the minimum and maximum peaking are used with the maximum PLL bandwidth. Previously only the maximum peaking was used. With this change, you may see a slight increase in Max HF RMS jitter in the range of ~10% or less reported in the Filter Compliance Summary section of the report.

## Version 4.2 [2020-02-24]

Improvements:

- Support Rohde & Schwarz waveform files
- Support larger waveform files

## Version 4.1 [2019-12-17]

Bug Fixes:

- Fixed: missing offset voltage in the Tektronics scope data. The user would not get the correct values when using Tektronics (.wfm) files in single-ended time-domain mode and the data would appear as if it was AC coupled.
- Fixed: waveforms that did not cross the rise and fall threshold would stop analysis with an error. Waveforms that do not cross the rise and fall threshold for the ERM will now skip this calculation.
- Fixed: peak-to-peak jitter calculation of clock inputs with spread spectrum enabled could have error. This did not affect PCIe compliance results. Expect changes only in the “pk-pk phase jitter” column.
- Fixed: GEN1 peak-to-peak phase jitter and compliance result was not reported.
- Fixed: if you opened a project file from explorer on a network drive and then tried to resave at the end of the wizard, the tool could crash.
- Fixed: fixed: filter compliance summary header typo: "Max HLF RMS -> Max LF RMS."
- Fixed: broken links on welcome screen.
- Hide PCIe 5.0 warning in footer of GUI on filter page.

Improvements:

- Added single-ended Clock Signals plot.
- Increased time vector resolution from 32-bits to 64-bits. This will reduce the arithmetical error do to the large range and small variation of the time array. This is particularly important for high sampling frequency scopes (above 50 GS/s).
- Changed threshold for time domain single ended crossing point detection. The ERM now follows the industry standard.

.NET 4.5 or higher is now required to install and run the PCIe Tool. Windows XP is no longer supported.

## Version 4.0 [2019-06-17]

- Refclock AC specification table improvements:
    - New symbol column matching the PCIe specification
    - Added $V_{IH}$ - differential Input High Voltage
    - Added $V_{IL}$ - differential Input Low Voltage
    - Added $V_{RB}$ - ring-back voltage
    - Added $V_{OVS}$ - overshoot voltage relative to $V_{IH}$
    - Added $V_{UDS}$ - undershoot voltage relative to $V_{IL}$

    - Added $F_{REFCLK}$ - Refclk Frequency
    - Added $F_{REFCLK\_32G}$ - Refclk Frequency for devices that support 32.0 GT/s
    - Added $F_{SSC}$ - SSC frequency range
    - Added $T_{SSC\text{-}FREQ\text{-}DEVIATION}$ - SSC deviation
    - Added $T_{SSC\text{-}FREQDEVIATION\_32G\_SRIS}$ - SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds
    - Added $T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$ - Max SSC df/dt
- New filter compliance summary at the top of the report. This summarizes test results for each class, data rate, architecture, and spec combination. Example:

| Class | Data Rate | Architecture | Specs | Max HF RMS | Max HLF RMS | Max Pk-Pk | Compliance Summary |
|---|---|---|---|---|---|---|---|
| GEN1 | 2.5 Gb/s | Common Clock | 1.1 2.1 3.1 | 2.85 ps | 1.17 ps | 27.37 ps | All PASS |
| GEN2 | 5 Gb/s | Common Clock | 1.1 2.1 3.1 | 2.21 ps | 649.64 fs | 7.44 ps | All PASS |
| GEN3 | 8 Gb/s | Common Clock | 3.1 4.0 | 719.26 fs | 85.03 fs | 1.84 ps | All PASS |
| GEN4 | 16 Gb/s | Common Clock | 4.0 | 719.25 fs | 85.03 fs | 1.82 ps | 18 FAIL |
| GEN5 | 32 Gb/s | Common Clock | 5.0 | 283.09 fs | 40.23 fs | 623.84 fs | 7 FAIL |
| GEN5 | 32 Gb/s | Separate Clock SRNS | 5.0 | 171.64 fs | 51.62 fs | N/A | N/A |
| GEN5 | 32 Gb/s | Separate Clock SRIS | 5.0 | 171.64 fs | 51.62 fs | N/A | N/A |

- New Waveform Analysis plots (when applicable):
    - Differential Clock Signal
    - Spread-Spectrum Clocking Profile
- Differential and single-ended time-domain inputs now support auto-threshold search for signals probed at mid-bus. The threshold value sets the best crossing point of the differential waveform to determine the TIE . The selected threshold will be included in the Differential Clock Signal plot in the compliance report.
- The ‘Reference-Clock-AC-Specs.csv’ file has new column ‘Symbol’
- The PCIeClockJitterTool command line interface (CLI) has a new option, --open-pdf, which will automatically open the compliance report after creation

## Version 3.0 [2018-12-12]

Bug Fixes

- Fixed: for the same device, the phase noise plot did not match the FFT of time domain plot (TMGSW-839)
- Fixed: when reading Le Croy data (.TRC), the period calculation had errors (TMGSW-856)
- Fixed: wrong H3 bandwidth for Gen2v4 (TMGSW-928)
- Fixed: updated sample filter transfer functions so that Gen2v4 CC plot is up-to-date (TMGSW-928)

General Improvements

- Changed spread spectrum spur removal to 2MHz for Gen4 and Gen5 (TMGSW-942)
- Added new phase noise datafile options:
    - Option to auto extend phase noise data to 50 Mhz (off by default) (TMGSW-837)
    - Support max folded frequency in phase noise analysis (on by default for new projects, off for any existing projects you open with this new version) (TMGSW-838)
- SRIS filters can now be enabled with phase noise data (TMGSW-836). Note that most phase noise analyzers do not support Spread Spectrum Clocks. Check if your equipment was able to properly lock to the center frequency before running this test.
- Spread Spectrum Phase Jitter Plot changes:
    - Time domain now in "s pp" instead of seconds
    - Phase noise remains in seconds; now exclude SSC Limit series as this does not apply
- Jitter plots have Y axis labels "Jitter (s pp)" and “Magnitude”

(version 3.0 release notes continued next page)

Filter Changes

- Added support for GEN5 SRNS
- Added overall H(s)=H1(s)*H3(s) to Gen3&4 SRIS
- Filter transfer function constant changes:
  - Omega constants for 2nd order functions are now calculated vs. truncated values
  - From this, some differences in Omega were found and corrected

| Filter | BW | Pk | Omega (old) | Omega (new) |
|---|---|---|---|---|
| CC Gen2 v4 H1 | 5000000 | 1 | 11010000 | 11459670 |
| CC Gen2 v4 H1 | 16000000 | 1 | 35260000 | 36670944 |
| CC Gen2 v4 H2 | 8000000 | 3 | 28860000 | 27039420 |
| DC Gen3 H3 | 10000000 | 2 | 33800000 | 30087861 |
| Gen5 SRIS H1 | 1800000 | 2 | 12040000 | 5415815 |
| Gen5 SRIS H2 | 1800000 | 2 | 12040000 | 5415815 |
| Gen5 SRIS H1 | 1800000 | 2 | 12040000 | 5415815 |
| Gen5 SRIS H2 | 1800000 | 2 | 12040000 | 5415815 |

  - Omega values change for other combinations, however significantly less (<0.1% to <0.6%)
  - You can use the new “Jitter Summary - Raw Data” comparison tool to review changes to compliance results that may result from this update
- Common clock improvements:
  - All possible bandwidth/peaking combinations are now calculated (TMGSW-840)
  - When BW/Peaking are different between H1(s) and H2(s), H and H’ values for BW/peaking are listed in the compliance report
  - For example, for Gen1 Common Clock, there are now three combinations shown instead of 1, as the case where H1(s) and H2(s) BW/peaking are equal is now calculated:

| # | Class | Data Rate | Arch (1) | Specs | PLL1 BW | PLL1 Peak | PLL2 BW | PLL2 Peak | CDR BW | CDR Peak | Specification | | | Analysis Result | | | Compliance Result |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | HF RMS | LF RMS | Pk-Pk | HF RMS | LF RMS | Pk-Pk | |
| 1 | GEN1 | 2.5 Gb/s | CC | 1.1<br>2.1<br>3.1 | 1.5 MHz | 3 dB | 1.5 MHz | 3 dB | 1.5 MHz | 0 dB | | | 86 ps | 118.40 fs | 12.04 fs | 968.38 fs | PASS |
| 2 | GEN1 | 2.5 Gb/s | CC | 1.1<br>2.1<br>3.1 | 1.5 MHz (H)<br>22 MHz (H') | 3 dB (H)<br>3 dB (H') | 22 MHz (H)<br>1.5 MHz (H') | 3 dB (H)<br>3 dB (H') | 1.5 MHz | 0 dB | | | 86 ps | 1.92 ps (H) | 190.38 fs (H) | 15.60 ps (H) | PASS |
| 3 | GEN1 | 2.5 Gb/s | CC | 1.1<br>2.1<br>3.1 | 22 MHz | 3 dB | 22 MHz | 3 dB | 1.5 MHz | 0 dB | | | 86 ps | 1.90 ps | 12.72 fs | 14.80 ps | PASS |

New ‘Jitter Summary - Raw Data.csv’ File Comparison/Aggregation Tools

- Two new tools can be used to compare/aggregate two or more 'Jitter Summary - Raw Data.csv' files. These CSV files summarize compliance test results and can be optionally saved using the 'Save Compliance Report Data' feature of the PCIe Clock Jitter Tool or the included PCIeClockJitterTool.exe Command Line Interface (CLI).
- Run the comparison from:
  - The PCIe Clock Jitter Tool welcome screen:

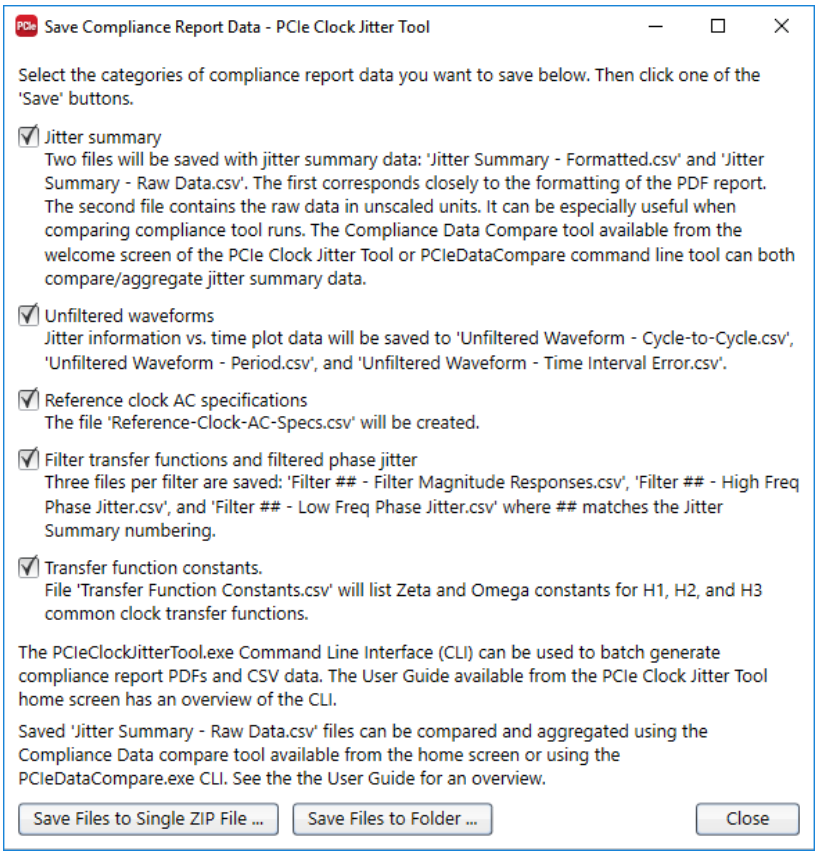

  - The new PCIeDataCompare command line tool; type PCIeDataCompare --help from the command line to learn more
- When two files are compared, jitter for each filter combination is compared and differences summarized. The PASS/FAIL compliance result for a filter combination is also summarized.
- When three or more files are compared, only the PASS/FAIL compliance result for each filter combination across all data files is summarized. Any number of files -- within the limits of PC memory and processing resources -- can be compared and the compliance results aggregated into a single report.

- The tool saves the comparison to an Excel workbook file.
- Here is a snippet from the Excel output when 3 CSVs were compared:

| Class | Data Rate | Arch | Specs | PLL1 BW | PLL1 Pk | PLL2 BW | PLL2 Pk | CDR BW | CDR Pk | Spec HF RMS | Spec LF RMS | Spec Pk-Pk | Result HF RMS #1 | Result H RMS #2 | | Result #1 | Result #2 | Result #3 | Result Summary |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GEN4 | 16 | CC | 4.0 | 2 | 0.01 | 5 | 0.01 | 10 | 0 | 0.5 | | | 0.526 | 0.3 | 41 | FAIL | PASS | PASS | 2 of 3 PASS |
| GEN4 | 16 | CC | 4.0 | 2 | 0.01 | 5 | 1 | 10 | 0 | 0.5 | | | 0.458 | 0. | 422 | PASS | PASS | PASS | 3 of 3 PASS |
| GEN4 | 16 | CC | 4.0 | 2 | 1 | 2 | 1 | 10 | 0 | 0.5 | | | | | 082 | | | PASS | 1 of 1 PASS |

Save Compliance Data Improvements

- What's New?
  - You can now select what compliance data to save
  - Compliance data now can be saved to folder in addition to ZIP
- How to Use
  - The "Save Compliance Report Data to ZIP" button on the compliance report screen of the GUI is now just "Save Compliance Report Data"
  - Clicking the button brings up this new form, where you can select what categories of data to save and then save to a ZIP file or a folder:




  - The PCIeClockJitterTool CLI has two new command line options:
    - --data-cats configures what categories to include. By default, all are.
    - --save-data-to-folder and --data-folder options are used to save compliance data to a folder (--create-data-zip and --data-zip-outfile are still available to save to ZIP)
  - Example:

```
PCIeClockJitterTool --file-type diff --wavefile wave.csv
                    --pdf-outfile report.pdf --data-folder compliance1
                    --data-cats summaries,waveforms
```

Only jitter result summary and the unfiltered waveform data will be saved to the folder "compliance1".

## Version 2.0 [2018-06-04]

- Fixed: SRIS and SRNS filter computation issue with phase noise data. The filter coefficients were corrected and RMS square sum applied to final jitter calculation.
- Fixed: in Jitter Summary CSVs generated by the “Save Compliance Report Data to ZIP” feature and CLI, the Compliance Result column was a single letter instead of PASS/FAIL
- Added support for Gen5 Common Clock and Separate Clock SRIS filters
- Added Reference-Clock-AC-Specs.csv to data file ZIP (time domain only)
- Added H(s) to Filter Magnitude Responses plots for SRIS and SRNS
- Excluded Gen3+ SRIS H3 Zeta/Omega from constants table due to transfer function complexity in these cases
- Updated Gen4 SRIS data rate
- Filter magnitude plots legend position changed
- Reworked how filters are defined and called: ~2x speedup of filter step
- Delay in overall transfer functions now via e^-sT instead of pade filter approximation
- Added information about aliased phase noise to the GUI and user guide

## Version 1.3 [ 2017-06-06 ]

- Fixed: if a jitter plot had a dense number of Y axis ticks, tick labels were skipped
- Changed Gen4 Common Clock HF RMS max from 1ps to 0.5ps
- Updated peaking and data rate for SRIS
- Added $s/(s+\omega_1)$ term to Gen3 v4.0 & Gen4 SRIS $H_s$ transfer functions
- When processing a phase noise waveform file, data below 1kHz is now ignored
- Added Gen3 v4.0 SRNS and SRIS filter results (in addition to keeping Gen3 v3.1 SRNS and SRIS)
- Added links to additional Skyworks app notes: AN781, AN946 and AN951

## Version 1.2 [ 2016-09-22 ]

- Fixed: clicking the Windows maximize button on the title bar would cause the tool’s bottom area, such as buttons, to be obscured by the taskbar
- Improved TIE analysis and detection of spread spectrum clocking.
- Improved SSC separation and post-FFT:
    - The bandwidth of frequencies removed (around the harmonics of the SSC frequency) was reduced to one-fifth the original bandwidth.
    - The interpolation post-SSC removal in this bandwidth was improved so that the interpolation reflects the true noise floor of the waveform.
- Added Gen4 SRNS and SRIS.
- Added new stand-alone SSC Phase Jitter plot to the compliance report.
- Changed PCIe v4.0 Gen1 max delay default to 12ns. Note that any existing project file will continue to use the delay present when last saved.
- Removed the 16MHz .5dB filter from Gen2 Data Clocked spec 3.1. Only the 16MHz 3dB filter is required.
- Gen2 SRNS and SRIS both showed H3 peaking of 0dB instead of 3dB. This has been fixed. The calculation was already correct.
- The edge filter and SSC separation options have been removed. Edge filtering is now always enabled. SSC separation is now always disabled for GEN1 filters and enabled for GEN2+. Any settings related to these in a previously saved project file will be ignored.
- References to BER have been removed from peak-to-peak phase jitter test captions. BER is not used to compute phase jitter: Pk-Pk = maxTIE – minTIE.

## Version 1.1 [ 2016-02-09 ]

- Installer digitally signed.
- Add SSC separation to all standards
- Fixed an issue where the SSC detection is inadvertently tripped to indicate no SSC even if box checked
- Fixed an SSC peak detection issue and increased the threshold to a more reasonable level.
- Changed the SSC separation replacement from rolling average to linear fit except in the case the linear fit has a negative slope in which case it uses a limited previous point average. This eliminates negative points in the dataset and looks reasonable in all the tests.
- Widened SSC separation frequency peak search range due to granularity issues with the low end spectrum. With only 160000 cycles, we can only have so much spectral data at 30Khz so a peak on the edge could be just a bit outside the 30-33KHz range

## Version 1.0 [ 2015-12-1 ]

Initial release.